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10/581,950	08/18/2008	Samuel S. Anderson	GWS-008	8737

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EXAMINER	
NGUYEN, DUY T V	
ART UNIT	**PAPER NUMBER**
2894	

NOTIFICATION DATE	DELIVERY MODE
06/16/2009	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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Office Action Summary	Application No.	Applicant(s)	
	10/581,950	ANDERSON ET AL.	
	Examiner	Art Unit	
	DUY T. NGUYEN	2894	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 May 2009*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-29 and 31-35* is/are pending in the application.

4a) Of the above claim(s) *1-8* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *9-29 and 31-35* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *07 June 2006* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *06/07/2006, 10/16/2008, 03/31/2009*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. Applicant's election without traverse of Group II, Species II (claims 9-29 and 31-35) in the reply filed on 5/22/2009 is acknowledged. Claims 1-8 are withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a nonelected invention. Claim 30 is canceled.

Drawings

2. The drawings are objected because of the following reasons:

Regarding Figures 5-8: please provide Figs. 5-8 as described in the specification.

Regarding Figure. 2: please add "2A" and "2B" for Figure 2, as described in the specification.

Figure 2 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Appropriate correction is required.

3. The drawings are objected to because "*copper pillar bump and copper direct (die) attach*" as claimed in claims 10, 19 and 25, are not shown. Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid

abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as “amended.” If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either “Replacement Sheet” or “New Sheet” pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Specification

4. The specification is objected because of the following reasons:

Regarding the specification: please add description for reference number “320”.

Appropriate correction is required.

Claim Objection

5. The claims are objected because of the following reasons:

Regarding claim 1, line 18: please replace "." with ";".

Regarding claim 10, lines 2: please delete “first” in front of copper.

Regarding claim 20, line 3: please delete a “said”.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

6. Claims 9, 12-29, and 31-35 are rejected under 35 U.S.C. 102(e) as being anticipated by Shen (US 6,972,464).

Regarding claim 9, Shen teaches, as shown in Fig. 1a, 1c and claim 1, a semiconductor device comprising:

a) a first doped region defined in a semiconductor substrate, said first doped region comprising a source (110) (col. 2, line 27);

b) a second doped region defined in said semiconductor substrate, said second doped region comprising a drain (120) (col. 2, line 28);

c) a first connectivity layer comprising a first runner (140) (col. 2, line 62) and a second runner (150) (col. 2, line 62), said first runner (140) being operatively connected to said first doped region (110) and said second runner (150) being operatively connected to said second doped region (120);

d) a second connectivity layer operatively connected to said first connectivity layer and comprising a third runner (160) (col. 3, line 15) and a fourth runner (170) (col. 3, line

25), wherein said third runner (160) being operatively connected to said first runner (140) and said fourth runner (170) being operatively connected to said second runner (150);

e) a third connectivity layer having comprising a first pad (180) operatively connected to said third runner (160) and a second pad (160) operatively connected to said fourth runner (170).

Regarding claims 12 and 13, Shen teaches said source is a source for a transistor and said drain is a drain for a transistor; and said source and said drain are laid out in a substantially enlongated shape and said source is interleaved with said drain (col. 3, lines 31-33, and Fig. 1a).

Regarding claim 14, Shen teaches a plurality of the sources and drains [0025].

Regarding claim 31, Shen teaches a plurality of said first pads and a plurality of said second pads (col. 4, lines 43-44 and claim 1).

Regarding claim 32, Shen teaches said first pad and said second pads are arranged in a substantially checkerboard pattern (col. 4, lines 43-44).

Regarding claim 33, Shen teaches said first sources and said second drains are arranged in a substantially checkerboard pattern (col. 4, lines 50-52).

Regarding claim 15, Shen teaches, as shown in Fig. 1a, a lateral discrete power MOSFET device comprising:

a) a first doped region defined in a semiconductor substrate, said first doped region comprising a source (110) (col. 2, line 27);

b) a second doped region defined in said semiconductor substrate, said second doped region comprising a drain (120) (col. 2, line 28);

c) a first connectivity layer,

where in a first portion (140) (col. 2, line 62) of the first conductivity layer is operatively connected to said first doped region (110) and a second portion (150) (col. 2, line 62) of the first conductivity layer being operatively connected to said second doped region (120);

Regarding claims 16 and 17, Shen teaches, as shown in Fig. 1a, a second connectivity layer (160) (col. 3, line 15) operatively connected to said first doped region (110) through said first connectivity layer (140); and said second connectivity layer (170) (col. 3, line 25) is operatively connected to said second doped (120) region through said first connectivity layer.

Regarding claim 18, Shen teaches, as shown in Fig. 1c, col. 3, lines 55-64, a third conductivity layer comprising a first pad and a second pad wherein said first pad is operatively connected to the first portion of said first connectivity layer and said second pad is operatively connected to the second portion of said first connectivity layer.

Regarding claim 19, Shen teaches, as shown in Figs. 1a and 1c, said first pad comprises a solder bump (184) (col. 3, line 43) and said second pad comprises a solder bump (194) (col. 3, line 62).

Regarding claim 20, Shen teaches a plurality of said first pads and a plurality of said second pads, wherein said first pad and said second pads are arranged in a substantially checkerboard pattern (col. 4, lines 43-44 and claim 1).

Regarding claim 21, Shen teaches said first pad is interleaved with said second pad (col. 4, lines 45-47).

Regarding claim 22, see claim 13 discussion.

Regarding claim 23, Shen teaches said source and said drain are laid out in substantially checkerboard pattern (col. 4, lines 51-52).

Regarding claim 24, Shen teaches, as shown in Figs. 1a and 1c, and claim 17, a lateral discrete power MOSFET device comprising:

a) a first doped region defined in a semiconductor substrate, said first doped region comprising a source (110) (col. 2, line 27);

b) a second doped region defined in said semiconductor substrate, said second doped region comprising a drain (120) (col. 2, line 28);

c) a first connectivity layer comprising a first runner (140) (col. 2, line 62) and a second runner (150) (col. 2, line 62), said first runner (140) being operatively connected to said first doped region (110) and said second runner (150) being operatively connected to said second doped region (120);

d) a second conductivity layer comprising a first pad operatively connected to said first runner and a second pad operatively connected to said second runner (col. 3, lines 55-64).

Regarding claim 25, Shen teaches, as shown in Figs. 1a and 1c, said first pad comprises a solder bump (184) (col. 3, line 43) and said second pad comprises a solder bump (194) (col. 3, line 62).

Regarding claim 26, Shen teaches a plurality of said first pads and a plurality of said second pads (col. 4, lines 43-44 and claim 1).

Regarding claim 27, Shen teaches said first pad is interleaved with said second pad (col. 4, lines 45-47).

Regarding claim 28, Shen teaches said source and said drain are laid out in a substantially enlongated shape and said source is interleaved with said drain (col. 3, lines 31-33, and Fig. 1a).

Regarding claim 29, Shen teaches a plurality of the sources and a plurality of the drains [0025].

Regarding claims 34-35, Shen teaches said first pad and said second pads are arranged in a substantially checkerboard pattern (col. 4, lines 43-44).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 10 and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shen in view of Applicant Admitted Prior Art (from hereinafter "Prior Art"). The teachings of Shen have been discussed above.

Regarding claim 10, Shen teaches first and second pads (see claim 9 discussion).

However, Shen fails to teach at least one of a copper pillar and a metal layer disposed thereon.

Prior Art teaches, as shown in Fig. 2B, at least one of a copper pillar and a metal layer [0013].

It would have been obvious to one of ordinary skill in the art at the time the invention was made to employ the teaching as taught by Prior Art in combination with Shen to have at

least one of a copper pillar and a metal layer disposed thereon because it aids in increasing electrical conductivity by using metallic material [0013].

Regarding claim 11, Shen teaches said first pad is interleaved with said second pad (col. 4, lines 45-47).

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

8. Claims 9, 10, 12, 14-19, 24-26, 29, and 31 are rejected under 35 U.S.C. 102(b) as being anticipated by Suzuki et al. (US 6,346,475, from hereinafter "Suzuki").

Regarding claim 9, Suzuki teaches, as shown in Fig. 2, a semiconductor device comprising:

a) a first doped region defined in a semiconductor substrate, said first doped region comprising a source (12) (col. 4, line 63);

b) a second doped region defined in said semiconductor substrate, said second doped region comprising a drain (14) (col. 4, line 63);

c) a first connectivity layer (first wiring layer, 42) (col. 5, line 25) comprising a first runner (40) (col. 5, line 17) and a second runner (40) (col. 2, line 62), said first runner (140) being operatively connected to said first doped region (12) and said second runner (40) being operatively connected to said second doped region (14);

d) a second connectivity layer (second wiring layer, 48) (col. 5, line 37) operatively connected to said first connectivity layer (40) and comprising a third runner (46) (col. 5, line 37) and a fourth runner (46), wherein said third runner (46) being operatively connected to said first runner (40) and said fourth runner (46) being operatively connected to said second runner (40);

e) a third connectivity layer having comprising a first pad (56) (col. 5, line 61) operatively connected to said third runner (46) and a second pad (56) ((col. 5, line 61) operatively connected to said fourth runner (46).

Regarding claim 10, Suzuki teaches each of first and second pads has at least on of a first copper pillar and a metal layer disposed thereon (see claim 4 and Fig. 2).

Regarding claim 12, Suzuki teaches said source is a source for a transistor and said drain is a drain for a transistor (col. 4, line 63).

Regarding claim 14, Suzuki teaches a plurality of the sources and drains (see Fig. 2).

Regarding claim 31, Suzuki teaches a plurality of said first pads and a plurality of said second pads (see Fig. 2).

Regarding claim 15, Suzuki teaches, as shown in Fig. 2, a lateral discrete power MOSFET device comprising:

a) a first doped region defined in a semiconductor substrate forming a source (12) (col. 4, line 63);

b) a second doped region defined in said semiconductor substrate forming a drain (14) (col. 4, line 63);

c) a first connectivity layer (first wiring layer, 42) (col. 5, line 25)

where in a first portion (42) of the first conductivity layer is operatively connected to said first doped region (12) and a second portion (42) of the first conductivity layer being operatively connected to said second doped region (14).

Regarding claims 16 and 17, Suzuki teaches, as shown in Fig. 2, a second connectivity layer (48) (col. 5, line 37) operatively connected to said first doped region (12) through said first connectivity layer (42); and said second connectivity layer (48) (col. 5, line 37) is operatively connected to said second doped region (14) through said first connectivity layer (42).

Regarding claim 18, Suzuki teaches, as shown in Fig. 2, a third conductivity layer (56) (col. 5, line 61) comprising a first pad and a second pad wherein said first pad is operatively connected to the first portion (42) of said first connectivity layer and said second pad is operatively connected to the second portion (52) of said first connectivity layer.

Regarding claim 19, Shen teaches, as shown in Fig. 2, said first pad comprises a copper direct attach (one of three layers of 56) and said second pad comprises a copper direct attach (one of three layers of 56) (see claim 4).

Regarding claim 24, Suzuki teaches, as shown in Fig. 2, a lateral discrete power MOSFET device comprising:

a) a first doped region defined in a semiconductor substrate, a first doped region defining a source (12) (col. 4, line 63);

b) a second doped region defined in said semiconductor substrate, a first doped region defining a drain (14) (col. 4, line 63);

c) a first connectivity layer (first wiring layer, 42) (col. 5, line 25) comprising first runner (140) being operatively connected to said first doped region (12) and a second runner (40) being operatively connected to said second doped region (14).

Regarding claim 25, Shen teaches, as shown in Fig. 2, said first pad comprises a copper direct die attach (one of three layers of 56) and said second pad comprises a copper direct die attach (one of three layers of 56) (see claim 4).

Regarding claim 26, Suzuki teaches a plurality of said first pad and a plurality of said second pads (see Fig. 2).

Regarding claim 29, Suzuki teaches a plurality of the sources and drains (see Fig. 2).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. Claims 11, 20, 21, 27, 32, 34 and 35 are rejected under 35 U.S.C. 103(a) as being unpatentable over Suzuki in view of Cheng (US 2003/0051217). The teachings of Suzuki have been discussed above.

Regarding claims 11, 21 and 27, Suzuki teaches said first pad and said second pad.

However, Suzuki fails to teach said first pad is interleaved with said second pad.

Cheng teaches, as shown in Fig. 2, said first pad is interleaved with said second pad.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to employ the structure as taught by Cheng in order to have first pad interleaved with second pad because it aids in reducing capacitance effects.

Regarding claims 20, 32, 34 and 35, Suzuki teaches a plurality of said first pad and a plurality of said second pads (see Fig. 2).

However, Suzuki fails to teach a checkerboard pattern.

Cheng teaches a checkerboard pattern (see Fig. 5).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to employ and modify structure as taught by Cheng in combination with Suzuki so that to have a first and second pads arranged in a substantially checkerboard pattern because it aids in reducing capacitance effects.

10. Claims 13, 22 and 28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Suzuki in view of Parker et al. (US 2003/0064574, from hereinafter "Paker"). The teachings of Suzuki have been discussed above.

Regarding claims 13, 22 and 28, Suzuki teaches said source and said drain (see claim 9 discussion).

However, Suzuki fails to teach a substantially elongated shape and said source is interleaved with said drain.

Parker teaches, as shown in Figs. 1-3, a substantially elongated shape and said source is interleaved with said drain [0014].

It would have been obvious to one of ordinary skill in the art at the time the invention was made to employ the teaching as taught by Parker in combination with Suzuki to have source and drain laid out in a substantially elongated shape and said source is interleaved

with said drain because it aids in providing a transistor device capable of handling a high currents [0002].

11. Claims 23 and 33 are rejected under 35 U.S.C. 103(a) as being unpatentable over Suzuki in view of Eden et al. (US 2002/0076851, from hereinafter “”Eden”). The teachings of Suzuki have been discussed above.

Regarding claims 23 and 33, Suzuki teaches said source and said drain.

However, Suzuki fails to teach a checkerboard pattern.

Eden teaches, as shown in Fig. 10, a checkerboard pattern.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to employ a checkerboard pattern as taught by Eden in combination with Parker to lay source and drain in substantially checkerboard pattern because it aids in reducing the inductance and resistance of electrical connection [0090].

Conclusion

12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to DUY T. NGUYEN whose telephone number is (571) 270-7431. The examiner can normally be reached on Monday-Friday, 7:30 Am - 5:00 Pm (alternative Friday Off).

If attempts to reach the examiner by telephone are unsuccessful, the examiner’s supervisor, Kimberly Nguyen can be reached on (571) 272-2402. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/DUY T NGUYEN/
Examiner, Art Unit 2894
6/2/2009

/Kimberly D Nguyen/
Supervisory Patent Examiner, Art Unit 2894